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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
Application Number				10/628,020	
Filing Date				July 25, 2003	
First Named Inventor				Yeo, <i>et al.</i>	
Art Unit				2811	
Examiner Name				TBD	
Attorney Docket Number				TSM03-0555	
Sheet	1	of	5		

U.S. PATENT DOCUMENTS					
Examiner Initials ¹	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
Cah	1	US-4,314,269	02-02-1982	Fujiki	
	2	US-4,631,803	12-30-1986	Hunter, et al.	
	3	US-4,946,799	08-07-1990	Blake, et al.	
	4	US-5,447,884	09-05-1995	Fahey, et al.	
	5	US-5,461,250	10-24-1995	Burghartz, et al.	
	6	US-5,534,713	07-09-1996	Ismail, et al.	
	7	US-5,629,544	05-13-1997	Voldman, et al.	
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	9	US-5,763,315	06-09-1998	Benedict, et al.	
	10	US-5,811,857	09-22-1998	Assaderaghi, et al.	
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	12	US-6,015,993	01-18-2000	Voldman, et al.	
	13	US-6,046,487	04-04-2000	Benedict, et al.	
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	16	US-6,232,163 B1	05-15-2001	Voldman, et al.	
	17	US-6,291,321 B1	09-18-2001	Fitzgerald	
	18	US-6,294,834 B1	09-25-2001	Yeh, et al.	
	19	US-6,387,739 B1	05-14-2002	Smith, III	
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	Cah	21	US-6,413,802 B1	07-02-2002	Hu, et al.
22		US-6,414,355 B1	07-02-2002	An, et al.	

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Examiner Signature	<i>Andrew M. ...</i>	Date Considered	12/02/04
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Yeo, et al.

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Signature**

Date Considered

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				Group Art Unit	2811
				Examiner Name	TBD
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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cita. No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	²
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	33	NAYAK, D.K., <i>et al.</i> , "Enhancement-Mode Quantum-Well Ge _x Si _{1-x} PMOS," IEEE Electron Device Letters, Vol. 12, No. 4, (April 1991), pp. 154-156.	
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	36	MIZUNO, T., <i>et al.</i> , "Novel SOI p-Channel MOSFETs With Higher Strain in Si Channel Using Double SiGe Heterostructures," IEEE Transactions on Electron Devices, Vol. 49, No. 1, (January 2002), pp. 7-14.	
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Examiner Signature	Andy Kung		Date Considered
			12/01/03

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Application Number	10/628,020
				Filing Date	July 25, 2003
				First Named Inventor	Yeo, <i>et al.</i>
				Group Art Unit	2811
				Examiner Name	TBD
Sheet	4	of	5	Attorney Docket Number	TSM03-0555

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
ah	45	MATTHEWS, J.W., <i>et al.</i> , "Defects in Epitaxial Multilayers – III. Preparation of Almost Perfect Multilayers," Journal of Crystal Growth, Vol. 32, (1976), pp. 265-273.	
	46	SCHÜPPEN, A., <i>et al.</i> , "Mesa and Planar SiGe-HBTs on MBE-Wafers," Journal of Materials Science: Materials in Electronics, Vol. 6, (1995), pp. 298-305.	
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	50	SHIMIZU, A., <i>et al.</i> , "Local Mechanical Stress Control (LMC): A New Technique for CMOS-Performance Enhancement," IEDM 2001, pp. 433-436.	
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ah	57	"Future Gate Stack," International Sematech, 2001 Annual Report.	
Examiner Signature			Date Considered
12/02/02			

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				Filing Date	July 25, 2003
				First Named Inventor	Yeo, <i>et al.</i>
				Group Art Unit	2811
				Examiner Name	TBD
Sheet	5	of	5	Attorney Docket Number	TSM03-0555

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite, No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	²
<i>ah</i>	58	CHANG, L., <i>et al.</i> , "Reduction of Direct-Tunneling Gate Leakage Current in Double-Gate and Ultra-Thin Body MOSFETs," 2001 IEEE, Berkeley, CA.	
<i>ah</i>	59	CHANG, L., <i>et al.</i> , "Direct-Tunneling Gate Leakage Current in Double-Gate and Ultrathin Body MOSFETs," 2002 IEEE, Vol. 49, No. 12, December 2002.	

Examiner Signature	<i>Andrew R. ...</i>	Date Considered	<i>12/02/03</i>
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<i>ah</i>	A	US-6,258,664 B1	07-10-2001	Reinberg	
	B	US-6,358,791 B1	03-19-2002	Hsu, <i>et al.</i>	
	C	US-2002/0153549 A1	10-24-2002	Laibowitz, <i>et al.</i>	
	D	US-6,475,838 B1	11-05-2002	Bryant, <i>et al.</i>	
	E	US-2003/0030091 A1	02-13-2003	Bulsara, <i>et al.</i>	
	F	US-6,524,905 B2	02-25-2003	Yamamichi, <i>et al.</i>	
	G	US-6,558,998 B2	05-06-2003	Belleville, <i>et al.</i>	
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FOREIGN PATENT DOCUMENTS						
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<i>ah</i>	H	WO 03/017336 A2	02-27-2003	Amberwave Systems Corporation		

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<i>ah</i>	I	WANG, L.K., <i>et al.</i> , "On-Chip Decoupling Capacitor Design to Reduce Switching-Noise-Induced Instability in CMOS/SOI VLSI," Proceedings of the 1995 IEEE International SOI Conference, Oct. 1995, pp. 100-101.	
<i>ah</i>	J	YEOH, J.C., <i>et al.</i> , "MOS Gated Si:SiGe Quantum Wells Formed by Anodic Oxidation," Semicond. Sci. Technol. (1998), Vol. 13, pp. 1442-1445, IOP Publishing Ltd., UK.	
<i>ah</i>	K	CAVASSILAS, N., <i>et al.</i> , "Capacitance-Voltage Characteristics of Metal-Oxide-Strained Semiconductor Si/SiGe Heterostructures," Nanotech 2002, Vol. 1, pp. 600-603.	

Examiner Signature	<i>Andrew H. Yeo</i>	Date Considered	12/10/03
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